

Appln No. 09/611,809
Amdt date November 28, 2005
Reply to Office action of September 28, 2005

REMARKS/ARGUMENTS

In the final Office action dated September 28, 2005 the Examiner rejected claims 1 - 4, 7 - 9, 12 and 14 - 27 under 35 U.S.C. § 103. Claims 1 - 4 and 9, 12 and 14 - 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hobson et al., U.S. Patent No. 6,209,016 (hereafter referred to as "Hobson") in view of Fischer et al., U.S. Patent No. 6,237,016) hereafter referred to as "Fischer"). Claims 7 and 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hobson in view of Fischer as applied to claim 1 and further in view of Curiger et al., U.S. Patent No. 6,064,740. Claims 1, 21 and 22 are independent. Claims 2 - 4, 7 - 9, 12, 14 - 20 and 23 - 27 depend on independent claim 1. Reconsideration and reexamination of claims 1 - 4, 7 - 9, 12 and 14 - 27 are hereby requested.

Applicant respectfully submits that the cited references do not teach or suggest the combination of claim 1 where an execution unit and a decode unit cooperate so that a determination is made as to whether a square operation or a product operation needs to be performed on an operand and, in response to that determination, the decode unit issues instructions to the execution unit so that when the square or product operations are performed, the execution unit performs specified multiplication and addition operations in parallel and performs specified multiplication operations in parallel.

In the Response to Applicant's Arguments, the Examiner cites Hobson at column 8, lines 28 - 30 as teaching the claimed use of instructions. Here, Hobson states that control of the sequence listed at column 8, lines 6 - 21 (sequence operations (1) - (9)) may be under software control using a CPU. The operations (1) - (5) and (7) are modular operations. Operation (6) is a simple subtraction operation. Operation (8) is a simple multiplication operation. Operation (9) is a simple addition operation.

The software of Hobson is thus merely used to control the order of the operations (1) - (9). No determination is made here as to "whether to perform a modular square or a modular multiply" as described by Hobson at column 6, lines 44 - 49. That determination is an entirely

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different part of the Hobson system. Accordingly, Hobson does not teach or suggest a decode unit that issues instructions based on such a determination.

In contrast, claim 1 relates to issuance of the instructions based on whether a square or product operation is to be performed. Here, the decode unit is used to determine if a square operation or a product operation needs to be performed on an operand and issues instructions so that an execution unit performs specified multiplication and addition operations in parallel and specified multiplication operations in parallel while performing either the square or product operation.

The Examiner also cites Fischer at columns 24 - 28 as teaching the claimed use of instructions. Specifically, the Examiner states that Fischer suggests "if/then statements and specific code operations in columns 24 - 28." Initially, Applicant has been unable to locate any if/then statements in the example code in columns 23 - 26 or in the claims at columns 25 - 28. Applicant therefore requests clarification of such statements.

Moreover, Applicant submits that Fischer also fails to teach the particularly claimed decode unit and execution unit of claim 1. Applicant has found no teaching or suggestion in Fischer that a decode unit issues instructions to an execution unit based on whether a square or product operation is to be performed so that the execution unit will perform specific operations in parallel while performing either the square or product operation.

Independent claims 21 and 22 include similar limitations relating to a decode unit determining whether a square or product operation is to be performed and issuing instructions so that simultaneous operations will be performed in response to those instructions.

In view of the above, Applicant respectfully submits that independent claims 1, 21 and 22 are not obvious in view of the cited art. Claims 2 - 4, 7 - 9, 12, 14 - 20 and 23 - 27 that depend on claim 1 also are patentable over the cited references for the reasons set forth above. In addition, these dependent claims are patentable over the cited references for the additional limitations that these claims contain.

For example, Applicant submits that the cited references do not teach or suggest performing multiplication and addition operations in parallel in a clock cycle as set forth, for

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example, in claims 23 and 24. The Examiner states in Response to Applicant's Arguments that "the "apparatus(es) disclosed in the cited art is capable of performing or being configured to perform the same functions."


Applicant has found no teaching in the references and no teaching has been cited by the Examiner that the claimed operations could be performed in a clock cycle as claimed. Rather, both of the cited references teach performing the operations in multiple cycles. For example, Fischer teaches at column 6, lines 13 - 15 that a multiply-accumulate operation requires two instructions. Hobson teaches that data is clocked and manipulated one or two bits at a time. See, for example, column 2, lines 28 - 48 (registers are "serially clocked one bit at a time" for multiplication operations and summing operations are performed "over the next 544 clock cycles") and column 4, lines 23 - 27 (the improvement involves processing two bits at a time per clock period) and column 5, lines 23 - 35 (the product is generated over 512 clock cycles). In the absence of any teaching regarding the specifically claimed operations, Applicant submits that the rejection of claims 23 and 24 is unwarranted.

CONCLUSION

In view of the above remarks, Applicant submits that the claims are patentably distinct over the cited references and that all the rejections to the claims have been overcome. Reconsideration and reexamination of the above Application is requested.

Respectfully submitted,

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